In the Claims

Claims 55-68, 79, and 80 are pending in the application with new claim 80 added herein.

Claims 1-54 (canceled).

55. (previously presented) An integrated circuit forming method comprising:

forming a first layer comprising copper for an integrated circuit over a substrate;

forming a second layer comprising a second metal different from copper over the first layer, the second metal comprising palladium;

incorporating at least some of the palladium into an intermetallic layer comprising the palladium and copper and having a thickness of from about 50 to about 150 Angstroms;

removing at least a portion of any second metal that is not incorporated into the intermetallic layer and exposing the intermetallic layer; and

forming a conductive connection for an integrated circuit directly to the intermetallic layer without a passivation layer therebetween.

56. (previously presented) The method of claim 55 wherein the intermetallic layer consists of copper and palladium.

57. (previously presented) The method of claim 55 wherein the incorporating comprises annealing the first and second layer at a temperature of greater than 400 to about 500 °C.

58. (previously presented) The method of claim 55 wherein the first layer has an elevational thickness before the incorporating, further comprising removing any second metal not comprised by the intermetallic layer, and any portion of the intermetallic layer, beyond the elevational thickness.

59. (previously presented) The method of claim 58 wherein the removing comprises chemical mechanical polishing.

60. (previously presented) The method of claim 55 wherein a rate of removing the second layer compared to the intermetallic material comprises greater than 5 to 1.

61. (previously presented) The method of claim 55 wherein the second layer consists of palladium.

62. (previously presented) An integrated circuit forming method comprising:

forming a first metal-containing material for an integrated circuit over a substrate;

forming a second metal-containing material over the first metal-containing material;

annealing the first and second metal-containing materials at a temperature of greater than 400 to about 500 °C to form an intermetal material from some of the first material and at least some of the second material, the intermetal material having a thickness of from about 50 to about 150 Angstroms; and

after the annealing, exposing the intermetal material to conditions effective to oxidize the first metal-containing material but the intermetal material protecting at least some of the first metal-containing material from oxidation during the exposing.

63. (previously presented) The method of claim 62 wherein the first metal-containing material consists essentially of copper, and the intermetal material consists of copper and palladium.

64. (previously presented) An integrated circuit forming method comprising:

forming a first level of integrated circuit wiring over a semiconductive substrate, the first wiring level comprising copper;

forming an intermetallic material at least partially within the first wiring level at a temperature of greater than 400 to about 500 °C, the intermetallic material comprising copper and palladium; and

forming a conductive via on and in electrical contact with the intermetallic material.

65. (previously presented) The method of claim 64 wherein the forming the intermetallic material comprises:

forming a layer comprising the palladium on the first wiring level;

annealing the layer and first wiring level; and

removing at least some of any palladium not comprised by the intermetallic material and leaving a sufficient thickness of intermetallic material to reduce oxidation of the first wiring level where the via connects to the first wiring level.

66. (previously presented) The method of claim 64 wherein the forming the conductive via further comprises forming a second level of integrated circuit wiring over the first wiring level during formation of the conductive via.

67. (previously presented) The method of claim 64 wherein the first level consists of copper.

68. (previously presented) The method of claim 64 wherein the intermetallic material consists of copper and palladium.

Claims 69-78 (cancelled).

79. (previously presented) An integrated circuit forming method comprising:

forming a first metal-containing material consisting essentially of copper for an integrated circuit over a substrate;

forming a second metal-containing material on and in contact with the first metal-containing material;

annealing the first and second metal-containing materials at a temperature of greater than 400 to about 500 °C to form an intermetal material from some of the first material and at least some of the second material, the intermetal material having a thickness of from about 50 to about 150 Angstroms and consisting of copper and palladium;

after the annealing, removing any of the second metal-containing material that is not incorporated into the intermetal material; and

after the removing, exposing the intermetal material to conditions effective to oxidize the first metal-containing material, but the intermetal material protecting the underlying first metal-containing material from oxidation during the exposing.

80. (new) The method of claim 55 further comprising, after the removing, exposing the intermetallic layer to conditions effective to oxidize the first layer, but the intermetallic layer protecting underlying portions of the first layer from oxidation during the exposing.